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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/655,695 | IOTOV, MIHAIL | |
| | Examiner | Art Unit | |
| | Dan Washburn | 2628 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/4/07 has been entered.

### *Response to Arguments*

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

### *Specification*

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification fails to provide proper antecedent basis for the term "computer-readable medium," which is described in claims 11-20.

### *Claim Objections*

Claims 6, 18, and 19 are objected to because of the following informalities: Claims 6, 18, and 19 all include amendments but the status of each claim is not 'currently amended'. The examiner does not feel that this warrants a notice of non-compliant amendment, but appropriate correction is required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over McDonald et al. (US 6,530,065) in view of Tojima et al. (US 6,898,771).

Regarding claim 1, McDonald describes a method for displaying timing data generated by simulating a circuit being designed by an EDA tool, the method comprising:

receiving the timing data from the EDA tool (column 5 line 16 through column 6 line 9 describes a server that provides simulation tools. A user gains access to the server computer through a web browser on a client computer and, once a user has created a functional circuit, the user runs the simulation, at which point the server computer runs the circuit simulation, generates output waveforms, and provides the output waveforms to the client computer so they can be displayed for a user. The server computer, and specifically the circuit simulation program running on the server computer, is considered the EDA tool. The waveform data that the client computer receives is considered timing data);

selecting first and second signals applied to nodes internal to the circuit based on input received from a user (column 11 line 38 through column 12 line 43 describes that

once a simulation is generated, a user may click on nodes or probes internal to the circuit in order to view waveforms at those points);

generating a first waveform for the first signal and a second waveform for the second signal using the timing data (Figure 5B and column 11 lines 38-55 describes that when a user clicks on nodes internal to the circuit the corresponding waveforms are displayed, which is considered generating waveforms);

displaying a portion of each of the first and second waveforms in an interactive graphical user interface, wherein the portion of each of the first and second waveforms displayed in the interface includes time points of interest to the user (column 12 lines 5-33 and Figure 5A describe a waveform of a node selected by a user. The waveform is displayed in an interactive window, and the window is part of the interactive graphical user interface illustrated in Figure 5B (multiple waveform windows may be displayed simultaneously). The waveform also includes data points represented as dots slightly larger than the rest of the graphed curve, which are considered time points of interest to the user);

displaying pointers to the time points of interest on the first and second waveforms (column 12 lines 5-43 describes that for a given waveform a user may place two markers on the waveform. The markers are labeled 'M1' and 'M2' and they are used to set a new start frequency and a new stop frequency for the waveform. Once M1 and M2 are set the client computer recalculates the magnitude, phase, frequency at magnitude equals 0, gain margin, and phase margin. The markers M1 and M2 are considered pointers to time points of interest (in this case the time points of interest are

the start and stop frequencies), where the markers can optionally be used on any waveform displayed by a user);

receiving edits to the time points of interest in response to a user moving the pointers on the interactive graphical user interface (Figure 5B and column 12 lines 5-43 describes that a user can set markers M1 and M2 to any values within the valid range of frequencies, which means a user can place M1 and M2, observe the recalculated values, and then move M1 and M2 in order to observe a second set of recalculated values, which is considered the client computer receiving edits to the time points of interest in response to a user moving the pointers on the interactive graphical user interface; and

updating circuit parameters based on the edits to the time points of interest to simulate the circuit (column 12 line 34 through column 13 line 8 describes that after a user has tested the behavior of the circuit under various conditions (where the circuit behavior is tested based on the edits to the waveforms) the user can alter the value of one or more of the circuit components by clicking on the components. Once the components have been updated the user can then initiate another simulation in order to observe the new waveforms, which is considered updating circuit parameters based on the edits to the time points of interest to simulate the circuit).

McDonald doesn't describe updating timing parameters of a circuit based on the edits to the time points of interest, in order to simulate the circuit.

However, Tojima describes updating timing parameters of a circuit based on edits to time points of interest on a waveform, in order to simulate the circuit (column 10

line 3 through column 11 line 20 and column 18 line 14 through column 19 line 7 describe that when a user designs a circuit the circuit may have inherent timing issues that are not obvious to the user. In the example given a user has designed an integrated circuit that comprises two integrated circuit blocks, the first block outputs a synchronization signal (sync-out) and a data signal (data-out), and the second block inputs the synchronization signal and the data signal. However, a timing issue exists in the circuit because the sync-out signal is output before the data on the data-out line is valid, which means the second block begins reading the data-out signal before the data is present on the input line. This problem is not obvious until a user generates a timing diagram that illustrates the behavior of the system. Once the timing diagram has been generated the user is able to determine that the sync-out signal should be delayed until the data on the data-out line is valid. In the described system the user is able to modify a signal waveform within the timing diagram in order to correct the issue. In this case the user can simply select and drag a waveform signal to the right in order to delay the signal by as many clock cycles as the user wishes. Once the waveform signal has been adjusted the system automatically converts the adjusted waveforms to functional elements that can be added to the circuit diagram in order to implement the change. The delay operation translates to a flip-flop that is added between the sync-out output of the first circuit block and the sync-in of the second circuit block, which has the effect of delaying the sync-out signal until the data on the data-out line is valid. The system automatically generating circuit elements and placing them in the circuit design based on changes a user makes to one or more waveforms in the timing diagram is

considered updating timing parameters of a circuit based on the edits to the time points of interest, in order to simulate the circuit).

All the elements of claim 1 are known in McDonald in view of Tojima, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in McDonald the system and method wherein a user is able to update timing parameters of a circuit based on edits to time points of interest, in order to simulate the circuit, as taught by Tojima, as this added functionality doesn't affect the overall operation of the rest of the system disclosed in McDonald, and it could be used to achieve the predictable result of a circuit simulation system that is able to simulate the behavior of an integrated circuit within a system, as well as the behavior of the utilized components within an integrated circuit, which increases the demand for the simulation system, as it applies to a wider range of design simulations.

RE claim 2, McDonald describes the method of claim 1 further comprising:

transmitting the updated circuit parameters back to the EDA tool (column 12 line 34 through column 13 line 8 describes that after a user sets markers M1 and M2 and the system recalculates the magnitude, phase, frequency at magnitude equals 0, gain margin, and phase margin, the user may interact with the simulation tool on the server computer in order to adjust the value of one or more of the circuit components. Thus, the user enters new values for one or more circuit components and runs a new simulation, which is considered transmitting the updated circuit parameters back to the EDA tool (which in this case is the simulation tool on the server computer));

generating updated first and second waveforms for the first and second signals using updated timing data received from the EDA tool, wherein the updated timing data is generated by simulating the circuit design using the updated circuit parameters (column 11 line 38 through column 12 line 42 describes that after a user enters new component values for one or more components and initiates a new simulation the user can click on one or more of the nodes within the circuit in order to display a waveform of the circuit behavior at that point, which is considered generating updated at least first and second waveforms (as there are at least two nodes within the circuit) for the first and second signals using updated timing data received from the EDA tool (the new output of the simulation tool on the server), wherein the updated timing data is generated by simulating the circuit design using the updated circuit parameters); and

displaying the updated first and second waveforms in the interactive graphical user interface (column 11 lines 38-55 describes that when a user selects a node of the circuit a waveform of the signal at that point is displayed).

McDonald doesn't describe transmitting the updated timing parameters back to the EDA tool.

However, Tojima describes a system and method wherein a user can modify a waveform and the system will automatically send this modification to an EDA tool, at which point the EDA tool will determine how to modify the circuit design in order to implement the new timing parameters (column 18 line 15 through column 19 line 7), which is considered transmitting the updated timing parameters (the modified waveform

data) back to the EDA tool (which in this case is the circuit design algorithm that alters the circuit schematic).

See the rejection of claim 1 for the rationale used to combine Tojima with McDonald, as the same rationale applies here.

RE claim 11, McDonald describes a computer-readable medium encoded with a computer program (column 20 lines 1-12 describe that the invention may be stored on a computer-readable medium), the computer program comprising a set of instructions for providing timing data generated by simulating a circuit being designed using an EDA tool, wherein the set of instructions when executed by a computer cause the computer to:

enable selection of signals applied to nodes internal to the circuit based on an input received from a user (column 11 lines 38-55 describes that a user may select signals applied to nodes internal to the circuit);

generate at least first and second waveforms for signals using the timing data (column 11 lines 38-55 describes that when a user selects a node in the schematic a waveform of the signal at that point is displayed (considered generating the waveform));

display a portion of each of the at least first and second waveforms in an interactive graphical user interface, wherein the portion of each of the at least first and second waveforms displayed in the interactive graphical user interface includes time points of interest to the user (column 12 lines 5-33 and Figure 5A describe a waveform of a node selected by a user. The waveform is displayed in an interactive window, and the window is part of the interactive graphical user interface illustrated in Figure 5B

(multiple waveform windows may be displayed simultaneously). The waveform also includes data points represented as dots slightly larger than the rest of the graphed curve, which are considered time points of interest to the user);

display pointers to the time points of interest on the waveforms (column 12 lines 5-43 describes that for a given waveform a user may place two markers on the waveform. The markers are labeled 'M1' and 'M2' and they are used to set a new start frequency and a new stop frequency for the waveform. Once M1 and M2 are set the client computer recalculates the magnitude, phase, frequency at magnitude equals 0, gain margin, and phase margin. The markers M1 and M2 are considered pointers to time points of interest (in this case the time points of interest are the start and stop frequencies), where the markers can optionally be used on any waveform displayed by a user);

generate new circuit parameters based on edits to the time points of interest received from the user, wherein the user moves the pointers on the interactive graphical user interface to generate the edits (Figures 5A and 5B and column 12 lines 5-43 describes that a user can change the location of M1 and M2 in order to adjust the start and stop frequency of the system, which is considered the user editing time points of interest (where the time points of interest are the start and stop frequencies). The system then automatically recalculates the magnitude, phase, frequency at magnitude equals 0, gain margin, and phase margin at this point based on the new start and stop frequencies, which is considered generating new circuit parameters based on the edits to the time points of interest);

generate updated waveforms for the signals using updated timing data, wherein the EDA tool generates the updated timing data by compiling, simulating and performing verification analysis on the circuit design using the new circuit parameters (column 11 line 38 through column 13 line 8 describes that a user can use the recomputed circuit parameters to make adjustments to the values of the circuit components. Once the user makes all the desired circuit component adjustments he initiates a new circuit simulation, which creates new waveforms, as the circuit behavior has changed. The user changing circuit values and running a new simulation is considered generating updated waveforms for the signals using updated timing data, wherein the EDA tool (the simulation tool on the server computer) generates the updated timing data by compiling, simulating, and performing verification analysis on the circuit design using the new circuit parameters); and

display the updated waveforms in the interactive graphical user interface (Figure 5B illustrates that a user can select a node within the circuit in order to display the updated waveform in the interactive graphical user interface (column 11 lines 38-55)).

McDonald doesn't describe updating timing parameters of a circuit based on the edits to the time points of interest, in order to simulate the circuit.

However, Tojima describes updating timing parameters of a circuit based on edits to time points of interest on a waveform, in order to simulate the circuit, as described in the rejection of claim 1. See the rejection of claim 1 for a complete discussion of how Tojima describes this limitation and for the rationale used to combine Tojima with McDonald, as the same rationale applies here.

RE claim 12, McDonald describes the computer-readable medium according to claim 11 wherein:

the display of the portion of each of the waveforms in the interactive graphical user interface further comprises display of each of the portions of the waveforms in synchronism (column 11 lines 38-55 describes that once a simulation is complete a user can click on nodes or probes indicated in the schematic to display waveforms, which is considered to include displaying the waveforms in the interactive graphical user interface in synchronism).

Claims 3, 4 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over McDonald et al. (US 6,530,065) in view of Tojima et al. (US 6,898,771), as applied to claims 1 and 11 above, and further in view of Liu et al. (US 6,662,126).

With regard to claims 3 and 14, McDonald in view of Tojima doesn't describe a method or computer readable medium wherein displaying the portion of each of the first and second waveforms in the interactive graphical user interface further comprises displaying a first waveform of a first clock signal received at a first storage element, and a second waveform of a second clock signal received at a second storage element.

However, Liu describes a system and method of measuring signal skew on a chip using on-chip sampling. Each on-chip sampler takes in an external signal and a global on-chip signal, and the samplers are compared to determine how much signal skew occurs as the signals propagate from one portion of the chip to a second portion of the chip (Figure 3 and column 3 lines 11-37). Further, Liu offers Figure 6, which

illustrates a timing diagram that describes how the skew of a global on-chip signal between two different points can be determined by using on-chip samplers. Figure 6 illustrates a first external modulated signal MOD_EXT_1 at a first point on the chip, an on-chip signal at the first point, CHIP_CLK_1, the same modulated signal at a second point on the chip, MOD_EXT_2, and the same on-chip signal at the second point, CHIP_CLK_2. The difference between these two signals, and the difference between both of these signals and the original input signals, describes a measurable amount of signal skew that occurs as a clock signal and an external signal propagate through the chip (column 7 lines 61-67 and column 8 lines 1-22). The on-chip samplers are described as being made up of transistors and inverters (column 4 lines 27-31), therefore the on-chip samplers are considered storage elements. It would have been obvious to one of ordinary skill in the art at the time of the invention to include in McDonald and Tojima the system and method of measuring a first waveform of a first clock signal received at a first storage element, and a second waveform of a second clock signal received at a second storage element, as taught by Liu, and displaying these measured waveforms on the interactive graphical user interface described by McDonald and Tojima, in order to allow a user to alter the timing of certain logical operations on the chip using the actual waveforms that the storage elements receive at their inputs, rather than the ideal clock waveform that doesn't account for signal skew. The advantage of allowing a user to work with the actual signals that each storage device receives at its input is that a user can fine tune the circuit timing to a very precise

level, as he can adjust for signal skew and other factors that can't be compensated for when working with an ideal clock signal.

As to claims 4 and 15, the combination of McDonald and Tojima doesn't describe a computer readable medium or method wherein displaying the portion of each of the first and second waveforms in the interactive graphical user interface further comprises displaying a third waveform of the first clock signal at first clock source, and a fourth waveform of the second clock signal at a second clock source, the first waveform of the first clock signal being delayed with respect to the third waveform by a first clock skew value, and the second waveform of the second clock signal being delayed with respect to the fourth waveform by a second clock skew value.

However, Liu describes a system and method of measuring the clock skew of an on-chip clock signal using an external signal and the global on-chip clock signal (column 3 lines 11-27, column 7 lines 61-67, and column 8 lines 1-22). Figure 3 illustrates two externally input signals, EXT and CHIP_CLK, and Figure 6 illustrates the signals as they appear at a first on-chip sampler (MOD_EXT_1, CHIP_CLK_1) and a second on-chip sampler (MOD_EXT_2, CHIP_CLK_2). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in McDonald and Tojima the system and method of measuring a waveform (considered a third waveform) of a first clock signal at a first source (EXT is considered a first clock signal), and measuring a waveform (considered a fourth waveform) of a second clock signal at a second source (CHIP_CLK is considered a second clock signal), where the first waveform (in this case MOD_EXT_1 or MOD_EXT_2) is delayed with respect to the third waveform by a first

clock skew value, and the second waveform (in this case CHIP_CLK_1 or CHIP_CLK_2) is delayed with respect to the fourth waveform by a second clock skew value, as taught by Liu, and displaying these measured waveforms on the interactive graphical user interface described by McDonald and Tojima, in order to allow the user to see exactly the extent of the signal skew that exists between the originally input signals and various points within a chip. The advantage of displaying the original signals along with the skewed signals is that a user can easily determine if the signal skew is unacceptably large at certain points on the chip and alter the design in order to correct the problem. Measuring and displaying signal skew allows a user to fine tune the circuit timing to a very precise level, as he can adjust for signal skew and other factors that can't be compensated for when working with an ideal clock signal.

With regard to claim 13, McDonald doesn't describe a computer-readable medium wherein the timing data generated by the EDA tool includes periods of a plurality of clock signals, duty cycles of the clock signals, offsets between the clock signals, and clock skews between sources of the clock signals and circuit elements that receive the clock signals.

However, Tojima describes a computer readable medium wherein the timing data generated by the EDA tool includes the period of a clock signal and the duty cycle of a clock signal (Figure 13A illustrates a clock signal that includes a period and a duty cycle). See the rejection of claim 1 for the rationale used to combine Tojima with McDonald, as the same rationale applies here.

The combination of McDonald and Tojima doesn't describe that the timing data generated includes a plurality of clock signals, duty cycles for a plurality of clock signals, offsets between the clock signals, and clock skews between sources of the clock signals and circuit elements that receive the clock signals.

However, Liu describes a computer readable medium that measures periods of a plurality of clock signals (EXT and CHIP_CLK, of Figure 3 are considered clock signals), duty cycles of clock signals (Figure 6 illustrates the measured clock signals at a first and second on-chip sampler, which includes the duty cycles of the measured clock signals), offsets between the clock signals, and clock skews between sources of the clock signals and circuit elements that receive the clock signals (Figure 6 illustrates MOD_EXT_1, CHIP_CLK_1, MOD_EXT_2, and CHIP_CLK_2, which are clock signals received at a first and second on-chip sampler, respectively, are offset from each other and from the original clock inputs, and are skewed signals with respect to each other and with respect to the original clock inputs (column 7 lines 61-67 and column 8 lines 1-22)). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in McDonald and Tojima the system of generating timing data that includes periods of clock signals, duty cycles of clock signals, offsets between the clock signals, and clock skews between sources of the clock signals and circuit elements that receive the clock signals, as taught by Liu. See the rejection of claims 3 and 14 for motivation to combine Liu with McDonald and Tojima, as the same motivation applies here.

Claims 5-10 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over McDonald et al. (US 6,530,065) in view of Tojima et al. (US 6,898,771) and further in view of Liu et al. (US 6,662,126), as applied to claims 3 and 15 above, and further in view of Pramanick et al. (US 2004/0216005).

Concerning claim 5, McDonald in view of Tojima and further in view of Liu doesn't describe a method wherein displaying the portion of each of the first and second waveforms in the interactive graphical user interface comprises displaying a launch edge of the first clock signal at which the first storage element releases a data signal, and displaying a latch edge of the second clock signal at which the second storage element captures the data signal.

However, Pramanick describes a method and system for testing timing related failures within an integrated circuit that includes a method wherein displaying the portion of each of the first and second waveforms in the interactive graphical user interface comprises displaying a launch edge of the first clock signal at which the first storage element releases a data signal, and displaying a latch edge of the second clock signal at which the second storage element captures the data signal (Figures 4B and 5A-5C and paragraphs 0043-0046 describe two flip-flops and their associated timing diagrams. Figure 5A illustrates that the input of the first flip-flop is driven high at 61, then at clk2 the input is latched into the first flip-flop (signal b at arrow 62), there is a bit of a propagation delay due to gate logic between the two flip-flops, and then the signal shows up at the input to the second flip-flop (signal c) and it is latched into the second flip-flop at clk3 (arrow 64). Signal b at arrow 62 is considered the launch edge of the

first clock signal at which the first storage element releases a data signal, and signal d at arrow 64 is considered the latch edge of the second clock signal at which the second storage element captures the data signal. These waveforms are presented to the user using the system described in Figure 6).

All the elements of claim 5 are known in McDonald, Tojima, Liu, and Pramanick, the only difference is the combination of known elements into a single system and method.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in McDonald, Tojima, and Liu the system and method wherein displaying the portion of each of the first and second waveforms in the interactive graphical user interface comprises displaying a launch edge of the first clock signal at which the first storage element releases a data signal, and displaying a latch edge of the second clock signal at which the second storage element captures the data signal, as taught by Pramanick, as displaying this particular circuit behavior doesn't change the operation of the system, and it could be used to achieve the predictable result of determining if the data being passed from one flip-flop to the next flip-flop has been on the data line long enough to allow the signal to stabilize before the receiving flip-flop attempts to latch it in. The advantage of this test is it allows a user to evaluate the integrity of each data signal as it is input into the receiving circuit module.

With regard to claim 6, McDonald in view of Tojima, and further in view of Liu doesn't describe a method wherein the interactive graphical user interface displays portions of the first waveform of the first clock signal and the second waveform of the

second clock signal that each start with a point in time corresponding to a period before both the launch and latch edges and end with a point in time corresponding to a period following both of those edges.

However, Pramanick describes a method wherein the interactive graphical user interface displays portions of the first waveform of the first clock signal and the second waveform of the second clock signal that each start with a point in time corresponding to a period before both the launch and latch edges and end with a point in time corresponding to a period following both of those edges (Figures 5A-5C all illustrate portions of the first and second waveforms that each start with clk1, which is considered at point in time corresponding to a period before both the launch and latch edges, and end at clk4 or unlabeled clk5 (the clock cycle after clk4) which is a point in time corresponding to a period following both of those edges).

See the rejection of claim 5 for the rationale used to combine Pramanick with McDonald, Tojima, and Liu, as the same rationale applies here.

As to claims 7, 16, and 17, McDonald describes a first time point of interest identified by a first one of the pointers on the interactive graphical user interface, and a second time point of interest identified by a second one of the pointers on the graphical user interface (column 12 lines 5-43 describes pointers M1 and M2).

McDonald, Tojima, and Liu don't describe that the launch edge of a waveform is the first time point of interest and the latch edge of the waveform is the second time point of interest.

However, Pramanick describes a system and method for testing timing related failures in an integrated circuit that includes monitoring the launch edge of a first storage element and monitoring the latch edge of a second storage element (Figures 4B and 5A-5C and paragraphs 0043-0046 describe two flip-flops and their associated timing diagrams. Figure 5A illustrates that the input of the first flip-flop is driven high at 61, then at clk2 the input is latched into the first flip-flop (signal b at arrow 62), there is a bit of a propagation delay due to gate logic between the two flip-flops, and then the signal shows up at the input to the second flip-flop (signal c) and it is latched into the second flip-flop at clk3 (arrow 64). Signal b at arrow 62 is considered the launch edge of the first clock signal at which the first storage element releases a data signal, and signal d at arrow 64 is considered the latch edge of the second clock signal at which the second storage element captures the data signal. These waveforms are presented to the user using the system described in Figure 6).

Given the description of manipulating a circuit design by adjusting pointers to time points of interest on a waveform disclosed in McDonald, and the teachings of manipulating a circuit design by adjusting the time between the launch edge of a first storage element and a latch edge of a second storage element, as disclosed in Pramanick, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in McDonald, Tojima, and Liu, the system and method wherein the launch edge of a waveform is the first time point of interest and the latch edge of the waveform is the second time point of interest, as taught by Pramanick, as this doesn't change the overall operation of the system suggested by McDonald, Tojima, and Liu,

and it could be used to achieve the predictable result of determining if the data being passed from one flip-flop to the next flip-flop has been on the data line long enough to allow the signal to stabilize before the receiving flip-flop attempts to latch it in. The advantage of this test is it allows a user to evaluate the integrity of each data signal as it is input into the receiving circuit module.

Regarding claim 8, McDonald in view of Tojima and further in view of Liu doesn't describe a method wherein updating the timing parameters based on the edits to the time points of interest further comprises updating a multi-cycle value that represents a number of active edges in the second clock signal between the launch edge and the latch edge.

However, Pramanick describes a method wherein updating the timing parameters based on the edits to the time points of interest further comprises updating a multi-cycle value that represents a number of active edges in the second clock signal between the launch edge and the latch edge (Figures 5B and 5C and paragraphs 0044-0046 describe that a user is able to alter the timing of the clock (considered a second clock signal) that two flip-flops operate off of in order to correct a timing error. In Figure 5B the propagation delay (delta bc2) between the launch edge of a first flip-flop and the latch edge of a second flip-flop is so large that a clock cycle passes before the value is ready to be latched by the second flip-flop. The logic that takes place between these two flip-flop operations is considered to have a multi-cycle value of one, as there is one active (positive) edge in the clock signal between the launch edge and the latch edge. A problem occurs at this point because the second flip-flop attempts to latch the

incoming value at clk3, but the value isn't ready, so the second flip-flop latches an incorrect value. In order to remedy this problem a user is able to alter the timing parameters of the clock during the propagation delay in order increase the period of the clock. The increased clock period gives the launch edge from the first flip-flop enough time to propagate through the required logic and arrive at the input of the second flip-flop before the next positive edge of the clock, which corrects the timing error. The multi-cycle value that represents a number of active edges in the clock signal between the launch edge and the latch edge has been updated from one to zero, as now there are zero active edges in the clock between the launch edge and the latch edge).

See the rejection of claim 5 for the rationale used to combine Pramanick with McDonald, Tojima, and Liu, as the same rationale applies here.

Concerning claims 9 and 10, McDonald doesn't describe a method wherein updating the timing parameters based on the edits to the time points of interest further comprises inverting the launch edge of the first clock signal, either in a design file or as an input to a static timing verification tool, nor does the combination describe a method wherein updating the timing parameters based on the edits to the time points of interest further comprises inverting the latch edge of the second clock signal.

However, Tojima describes a method wherein updating the timing parameters based on edits to the time points of interest further comprises inverting displayed waveforms, which is considered to include inverting the logic that controls the launch edge and latch edge for storage devices (Figures 13A and 13B and column 18 lines 20-51 describes that a user may double-click on a waveform in order to invert the entire

signal). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in McDonald the method of inverting the launch edge of a clock signal and inverting the latch edge of a clock signal, as taught by Tojima, in order to test the performance of a circuit using negative logic, where the flip-flops launch and latch values based on the negative edges of a clock signal. The advantage of testing a circuit using negative logic is that a user can see how the circuit reacts to a wider range of tests, which helps create a more robust design.

As to claims 18 and 19, McDonald describes a first time point of interest identified by a first one of the pointers on the interactive graphical user interface, and a second time point of interest identified by a second one of the pointers on the graphical user interface (column 12 lines 5-43 describes pointers M1 and M2, each displayed waveform optionally includes pointers M1 and M2, which means first, second, third, and fourth pointers can potentially exist (as long as at least two waveforms are displayed)).

Further, McDonald in view of Tojima suggests a computer that generates new timing parameters based on the edits to time points of interest, where the user edits the time points of interest by moving the first or second pointer on the interactive graphical user interface, as described in the rejection of claims 1 and 11.

McDonald in view of Tojima and further in view of Liu doesn't describe a computer-readable medium wherein the computer generates the new timing parameters based on the edits to the time points of interest by changing a multi-cycle value that represents a number of active edges in the second clock signal from the launch edge to

the latch edge in response to the user moving the first or second pointer on the interactive graphical user interface.

However, Pramanick describes a computer readable medium wherein the code for generating the new timing parameters based on the edits to the time points of interest further comprises code for changing a multi-cycle value that represents a number of active edges in the second clock signal from the launch edge to the latch edge, as described in the rejection of claim 8.

Given the description of manipulating a circuit design by adjusting pointers to time points of interest on a waveform disclosed in McDonald in view of Tojima, and the teachings of manipulating a circuit design by adjusting the time between the launch edge of a first storage element and a latch edge of a second storage element, as disclosed in Pramanick, it would have been obvious to one of ordinary skill in the art at the time of the invention to include in McDonald, Tojima, and Liu, the system and method wherein the system generates new timing parameters by changing a multi-cycle value that represents a number of active edges in the second clock signal from the launch edge to the latch edge, as taught by Pramanick, as this doesn't change the overall operation of the system suggested by McDonald, Tojima, and Liu, and it could be used to achieve the predictable result of determining if the data being passed from one flip-flop to the next flip-flop has been on the data line long enough to allow the signal to stabilize before the receiving flip-flop attempts to latch it in. The advantage of this test is it allows a user to evaluate the integrity of each data signal as it is input into the receiving circuit module.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over McDonald et al. (US 6,530,065) in view of Tojima et al. (US 6,898,771), as applied to claims 1 and 11 above, and further in view of Chan (US 6,466,898).

The combination of McDonald and Tojima doesn't describe a computer readable medium wherein the circuit design is a design for a field programmable gate array.

However, the background of Chan describes that a logic simulator is an essential electronic design automation (EDA) tool to facilitate the design and debug of very large scale integrated circuits (column 1 lines 5-20). The background of Chan further describes that some EDA vendors have hardware-accelerators or hardware emulators, where the hardware emulators program field programmable gate array (FPGA) chips (column 2 lines 4-23). It would have been obvious to one of ordinary skill in the art at the time of the invention to include in McDonald and Tojima the system of using the EDA tool and timing analyzer to program an FPGA, as taught by the background of Chan, in order to apply the system taught by McDonald and Tojima to debugging and programming FPGA chips, which increases the market demand for the system, as an FPGA chip is a common and popular chip to work with for commercial and educational purposes.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Washburn whose telephone number is (571) 272-5551. The examiner can normally be reached on Monday through Friday 8:30 a.m. to 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on (571) 272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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